REMARKS

The Office Action dated January 23, 2006 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. No claims have been amended, and no new matter has been introduced. Claims 1-7 are pending and are submitted for consideration.

Claims 1-2, and 7 stand rejected under 35 U.S.C. 102(a) as being unpatentable over *Muller* (U.S. Patent No. 5,909,686), hereinafter referred to as *Muller I.* The Office Action took the position that *Muller I* teaches each and every element recited in claims 1, 2, and 7. Applicants traverse the rejection and respectfully submit that *Muller I* does not teach or disclose each and every element recited in claims 1, 2, and 7.

Claim 1, upon which claims 2-4 and 6 are dependent, recites a network switch stack configuration, said configuration comprising a first network switch comprising a plurality of data ports, a first stacking port, a first internet port interface controller, and a first CPU interface, a second network switch having a plurality of data ports, a second stacking port, a second internet port interface controller, and a second CPU interface, and a common CPU connected to said first CPU interface and said second CPU interface, wherein the first stacking port and the second stacking port are communicatively connected through said first and second internet port interface controllers, such that incoming packets on any of the plurality of data ports on the first and second switches are effectively switched to any of the plurality of data ports on either of the first and second

network switches, and wherein the first switch adds a module headers having module identifier fields, providing a source module ID of the first switch, to the incoming packets and the second stacking port reads the module headers to determine egress ports for the packets.

Claim 7 recites a method for routing packets in a network switch stack configuration, the method comprising communicatively connecting a first stacking port and a second stacking port, wherein a first network switch includes said first stacking port and a second network switch includes said second stacking port, adding module headers having module identifier fields, providing a source module ID of the first switch, to incoming packets on any of a plurality of data ports by said first switch, reading the module headers by the second stacking ports to determine egress ports for said incoming packets, and switching said incoming packets to said egress ports via at least one internet port interface controller, said egress ports including any of the plurality of data ports on either of the first and second network switches.

Muller I teaches a method and apparatus for providing hardware-assisted CPU access to a forwarding database. A switch fabric provides access to a forwarding database on behalf of a processor, and includes a memory access interface configured to arbitrate access to a forwarding database memory. The switch fabric includes interfaces for communicating with a CPU, shared memory, network ports and a cascading interface communicating with one or more switch elements.

However, *Muller I* does not teach or disclose that each network switch in the stacked switch configuration contains an internet port interface controller (IPIC), as recited in independent claims 1 and 7. The IPIC recited in independent claims 1 and 7 is recited as being positioned between the stacking ports of the respective switches, *i.e.*, the first stacking port and the second stacking port are "communicatively connected through the first and second internet port interface controllers." Referring to Figure 2 of *Muller I* and the associated discussion thereof at columns 2-4, Applicants note that no IPIC is shown between the stacking ports 225 of the respective switches. In fact, the stacking port 225 is the last element that must be traversed by data when leaving a first switch and being transmitted to a second switch. Given that there are no additional elements shown or discussed in the transmission path after the stacking port 225, it is clear that *Muller I* does not teach or disclose an IPIC being positioned between the stacking ports. Therefore, Applicants submit that *Muller I* fails to teach or disclose each and every element recited in independent claims 1 and 7. As such, reconsideration and withdrawal of the rejection of claims 1 and 7, along with dependent claim 2, is respectfully requested.

Further supporting Applicants position that *Muller I* does not teach the IPIC recited in independent claims 1 and 7, Applicants point to the discussion of the IPIC on page 103 of the application at the paragraph beginning with "Figure 28 is an overview of the functional elements of an IPIC 90." The exemplary IPIC is described as including tables 91, a network buffer pool (NBP) 92, and arbiter 93, and flow control logic 94. *Muller I* does not teach any sort of an IPIC having these components, wherein the first

stacking port and the second stacking port are communicatively connected through the IPICs of the first and second switches. Therefore, Applicants submit that *Muller I* fails to teach or disclose each and every element recited in independent claims 1 and 7. As such, reconsideration and withdrawal of the rejection of claims 1 and 7, along with dependent claim 2, is respectfully requested.

Further, Applicants note that it is well established in US Patent Law that in order for a §102 rejection to be proper, the reference cited in support of the §102 rejection must teach each and every element recited in the rejected claim. Further, it is also well established that, when making a prior art rejection, the Office has the responsibility of indicating to the Applicants what elements of the reference(s) are anticipatory. In this case, Applicants submit that the Office Action has not properly supported the §102 rejection, as the Office Action does not indicate what elements described in *Muller* correspond to the elements recited in the rejected claims. More particularly, Applicants note that the Office Action does not in any way indicate what element of *Muller I* is equivalent to the IPIC recited in Applicants independent claims 1 and 7. Applicants submit that the *Muller I* does not teach the IPIC recited in Applicants' claims, however, if the Office Action disagrees, citation to an element in *Muller I* this anticipates the recited IPIC is respectfully requested. Absent such a citation, Applicants submit that *Muller I* clearly fails to teach or disclose the IPIC, and reconsideration and withdrawal of the rejection is respectfully requested.

Further still, as noted above, the references cited in support of a §102 rejection must teach each and every element recited in the rejected claim. The Office Action, on page 3 draws the broad conclusion that since *Muller I* discloses Ethernet packet switches, then "each of the switch elements 100 in the system shown in Figure 1 adds to each of the incoming data packets a Ethernet header, which comprises a plurality of header fields." However, the Office Action does not indicate any particular citation to a column or paragraph of *Muller I* that supports this broad conclusion. Applicants submit that upon careful consideration of *Muller I*, a more accurate conclusion would be that although the reference indicates that packet headers are present and are read and parsed by the switches, there is no teaching or disclosure that the packet headers have a module ID field added to the header by the first network switch, as recited in independent claims 1 and 7. Therefore, Applicants submit that *Muller I* fails to teach or disclose each and every element recited in claims 1 and 7, and as such, reconsideration and withdrawal of the rejection of claims 1 and 7, along with dependent claim 2, is respectfully requested.

Claims 3-6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over *Muller I* in view of *Muller* (U.S. Patent No. 6,119,196), hereinafter referred to as *Muller II*. The Office Action took the position that *Muller I* teaches each and every element recited in claims 306, except for the cascading interface including an arbiter. However, the Office Action noted that *Muller II* teaches an arbiter, and as such, the Office Action concluded that it would have been obvious for one of ordinary skill in the art to combine the teaching of the references to generate the claimed invention. Applicants traverse the

rejection and respectfully submit that the cited combination of references fails to teach, show, or suggest each and every element recited in claims 3-6.

Claims 3-6, which depend from claim 1, recite the following: Claim 3 recites a network switch stack configuration as recited in claim 1, wherein each of said first and second stacking ports include an arbiter thereupon, for allocating communication bandwidth between the first and second stacking port; Claim 4 recites network switch stack configuration as recited in claim 1, wherein each of said first and second stacking ports includes flow control logic for controlling data flow to and from each of the first and second network switches, respectively; Claim 5 recites a network switch stack configuration as recited in claim 3, wherein each arbiter is configured to alternate bandwidth access by alternating transmission and reception of data based upon a predetermined algorithm; and claim 6 recites a network switch stack configuration as recited in claim 1, wherein the first and second stacking ports are configured to forward the packets to the egress ports without requiring a lookup in an address resolution table.

Muller I is discussed above. *Muller II* teaches method and apparatus for managing a buffer memory in a packet switch that is shared between multiple ports in a network system. The apparatus comprises a plurality of slow data port interfaces configured to transmit data at a first data rate between a slow data port and the buffer memory and a plurality of fast data port interfaces configured to transmit data at a second data rate between a fast data port and the buffer memory. A first level arbiter is coupled to the

plurality of slow data port interfaces, where the first level arbiter chooses an access request of one the slow data ports and outputs the access request.

As a preliminary matter, Applicants note that each of claims 3-6 depend from claim 1, which has been presented above as allowable. Therefore, Applicants submit that claims 3-6 are also allowable as a result of being dependent upon an allowable base claim. Reconsideration and withdrawal of the rejection is respectfully requested.

However, Applicants note that *Muller II* also does not teach an internet port interface controller, as recited in independent claims 1 and 7. Since neither *Muller I* or *Muller II* teach this feature that is expressly recited in Applicants independent claims, Applicants submit that the cited combination of references fails to teach, show, or suggest each and every limitation recited in independent claims 1 and 7. Therefore, reconsideration and withdrawal of the rejection of independent claims 1 and 7, along with dependent claims 2-6, is respectfully requested.

Further, aside from neither of the *Muller* references teaching the IPIC recited in the rejected claims, Applicants submit that the combination of references still fails to teach, show, or suggest each and every element recited in Applicants' claims. More particularly, claim 3 expressly recites that the arbiter is positioned in the stacking ports. As acknowledged by the Office Action at the end of page 4 through the beginning of page 5, neither of the *Muller* references teach that the arbiter is positioned in the stacking port. Since the structural position of the arbiter is expressly recited in claim 3, a proper rejection under §103 must show a reference that teaches, shows, or suggests that the

arbiter taught by *Muller II* could be combined into the stacking port taught by *Muller I*. Applicants submit that there is no such teaching or showing to be found in either of the *Muller* references. As such, reconsideration and withdrawal of the rejection of claim 3 is respectfully requested.

Further, it is well known that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention, where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves, or in the knowledge generally available to one of ordinary skill in the art. *See*, In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). In the instant case, the Office Action has merely stated that it would have been obvious to one of ordinary skill in the art to combine the arbiter from *Muller II* into the stacking port of *Muller I*, without citing to any particular section from either of the references that illustrates that one of ordinary skill in the art would have been motivated to combine the references in this manner. Further, the Office Action has not presented any support for the conclusion that one of ordinary skill in the art would have known to combine the teaching of the references at the time the instant application was filed, or more particularly, to combine the references in the particular structural configuration recited in claim 3 (the arbiter positioned in the stacking port). Rather, the Office Action has merely drawn a broad conclusion that one of ordinary skill in the art could have combined the references to generate the claimed invention.

Applicants note that M.P.E.P. §2143.01 states that the mere fact that references *can* be combined or modified does not render the resultant combination obvious *unless the prior art also suggests the desirability of the combination*. *See*, In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990). (*Emphasis added*) In the instant case, Applicants submit that there is no teaching or suggestion either in the references themselves or in the knowledge available to one of ordinary skill in the art at the time the application was filed to incorporate the arbiter from *Muller II* into the stacking port of *Muller I*. As such, when the Office Action fails to provide specific motivation to combine references, the Federal Circuit, the Board, and the M.P.E.P are clearly aligned in taking the position that "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." *See*, M.P.E.P § 2141 and Hodosh v. Block Drug Co., Inc. 786 F.2d 1136, 229 USPQ 182 (Fed. Cir. 1986). In view of the lack of teaching and motivation, reconsideration and withdrawal of the rejection of claim 3, along with claim 5 which depends therefrom, is respectfully requested.

With regard to the rejection of claim 4, Applicants submit that the cited combination of references fails to teach the flow control logic recited in the claim. More particularly, the Office Action takes the position that the buffer memory controller (BMC) discussed in *Muller II* is equivalent to the flow control logic recited in claim 4. Applicants submit that the conclusions drawn in the Office Action are misplaced. The flow control logic recited in claim 4 is not simply a memory controller. Rather, as

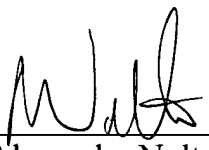
described in the specification at pages 62-63 and 70-75, the flow control logic is more than a buffer memory controller that simply controls access to a memory, the flow control logic operates to check bits in the packet header and control packet flow. This feature is not taught by either of the *Muller* references, and as such, reconsideration and withdrawal of the rejection is respectfully requested.

In conclusion, Applicants submit that each of claims 1-7 recite subject matter that is not taught, shown, or other wise suggested by either of the *Muller* references, taken either alone or in combination. Therefore, Applicants submit that claims 1-7 are allowable over the cited art, and reconsideration and withdrawal of the rejection is respectfully requested. Claims 1-7 are pending and are submitted for consideration.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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